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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/779,807 | 02/18/2004 | Christopher Edwin Wrigley | 550-526 | 6827 |

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| EXAMINER | |
|---|---|
| UNELUS, ERNEST | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2181 | |

DATE MAILED: 12/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/779,807 | WRIGLEY ET AL. | |
| | Examiner | Art Unit | |
| | Ernest Unelus | 2181 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on *29 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) *1-12,17-27 and 32* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-16 and 28-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
12/6/2006

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

## RESPONSE TO AMENDMENT

Applicant's arguments filed 09/29/2006 have been fully considered but they are not persuasive.

**Response based on traversed restriction requirement**

**Applicant argues that claim 13 is generic. As discloses in MPEP 806.04(d) "A Generic Claim in an application presenting three species illustrated, for example, in Figures 1, 2, and 3, respectively, a generic claim should read on each of these views". Claim 13 or 28 do not read on, for example, claim 1, which is directed towards fig. 9, because, while claims 13 and 28 required one bus, claim 1 requires two different buses. Fig. 9 discloses two different buses, while, base on the language of claims 13 or 28, the bus must be a single bus.**

**Claim rejections based on prior art**

**The applicant argues that the cited Minami reference doesn't discloses "a single read/write port which has both a read channel and a write channel and that these two channels can operate and perform data reads and writes independently of each other". The applicant's fig. 3 discloses a single port 47, which clearly has a read input 47A and a write output 47C, which are not the same. Similarly, Minami's fig. 3 shows a connection (read port) between the system bus and the DMA and a connection (write port) between the DMA and an I/O device. Therefore, Minami's read and write ports are also independent of each other. In col. 1, lines 22-26, Minami discloses "*In one function, the DMA controller causes the I/O device to output data and writes the data into the main storage. In the other***

*function, the DMAcontroller reads out data from the main storage and causes the I/O device toreceive the data*"

**The claim language does not discloses a physical structure of the port and doesn't require simultaneously independent, only independent. Also, the claim only requires the channels to be "operable" to receive and output.**

## I. RESPONSE TO THE APPLICANT'S ELECTION

1. Applicant's election with traverse of Species I in Figures 3 and 7 mailed May 5, 2006 (Paper No. 05052006) in the reply filed on June 05, 2006 is acknowledged. The traversal is on the ground(s) that "*Species II illustrated in Figure 5 is a subset of Figure 3, i.e. splitting the single register 45 into two separate registers 45A and 45B. Additionally, Applicants contend that the Examiner's alleged Species II as disclosed in Figure 8 is actually the same species as Figure 3*". **This is not found persuasive because Species II illustrated in figure 5 shows two separate registers 45A and 45B, which is a different embodiment from Species I. Species I and III are different. Species I shows a register inside the DMAC while Species III discloses a DMAC without a register. The applicant's argument is not convincing because the applicant's specification doesn't support the argument. The Applicant's "Brief Description Of The Drawings" discloses Figure 5 as an embodiment and not a subset of figure 3, which is a different embodiment from Figure 5. Page 11 on the applicant's specification also stated "*FIG. 5 shows a DMAC similar to that shown in FIG. 3, but in this case there are two storage registers in parallel*". Figures 5 and 3 are similar. However, similar doesn't mean the same or a subset.**

**The applicant also argued that Species III as disclosed in Figure 8 is actually the same species as Figure 3. Species III is not the same species as figure. They are different for the same reason stated above, which is different embodiment, as disclosed in the applicant's drawing and specification.**

The requirement is still deemed proper and is therefore made FINAL.

Claims 1-12 and 17-27, and 32 withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected Species IV, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on June 05, 2006. Thus, at this point claims 13-16 and 28-31 are ready for examination by the examiner.

## II. INFORMATION CONCERNING OATH/DECLARATION

***Oath/Declaration***

2. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63.**

## III. INFORMATION CONCERNING DRAWINGS

***Drawings***

3. The applicant's drawings submitted are acceptable for examination purposes.

## IV. ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

4. As required by M.P.E.P. 609(C), the applicant's submissions of the Information Disclosure Statement dated September 21, 2005 is acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by M.P.E.P 609 C(2), a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

## V. REJECTIONS BASED ON PRIOR ART

### *Claim Rejections - 35 USC § 102*

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. **Claims 13-16, and 28-31,** are rejected under 35 U.S.C. 102(e) as being anticipated by Minami (US pat. 6,651,114).

7. As per **claims 13 and 28**, Minami discloses "A direct memory access controller **(DMAC 280 in fig. 3)** for controlling data transfer between a data source **(RAM 220 in fig. 3)** and a data destination **(I/O device 240 in fig. 3)** comprising: a single read/write port **(the read/write port between the bus and the DMAC in fig. 3)** comprising a read channel operable to receive data from said data source via a read path on a bus and a write channel operable to output said received data to said data destination via a write path on said bus **(col. 1, line 67 to col. 2, line 5 discloses "data itself is read from or written into the main storage (RAM) 220 through the system bus 200 and a bus interface of the DMA controller 280. Further, the data is transferred between the DMA controller 280 and the I/O devices 240, 250 and 260 through the I/O bus 270")**, said read and write channel being operable to perform data reads and writes independently of each other" **(col. 1, lines 23-26 discloses "the DMA controller has two functions. In one function, the DMA controller causes the I/O device to output data and**

**writes the data into the main storage. In the other function, the DMA controller reads out data from the main storage and causes the I/O device to receive the data").**

8. As per **claims 14 and 29**, Minami discloses "A direct memory access controller according to claim 13," **[see rejection to claim 13 above]** said direct memory access controller further comprising control logic **(page 2 from the applicant's specification sated "*Furthermore control logic in state machines are required to control the sequencing of the transfer of data from the source to the FIFO and from the FIFO to the destination*". Similarly, Minami discloses "In a case where data transfer is made while performing hand shaking using the two signals Req* and Ack* between the DMA controller and the I/O device in the above-stated manner, the data transfer rate obtainable by a perfect-synchronized-type design can be suppressed at the most to a transfer rate of "(I/O bus width).times.(system clock signal frequency).times.1/2", which is a control logic to transfer data between the source and the destination; see col. 3, lines 25-32)**, said control logic being operable: to generate a source control signal specifying at least one data transfer from said data source **(Minami discloses in fig. 2 a control line 170. As it known in the art, control lines are used to carry control signal. This control line is being used to specify a data transferred from the RAM 120 to one of the destination I/O devices)**, said read/write port further comprising a control channel **(col. 3, lines 5-40 discloses control channel to transfer data between a RAM and an I/O device, which take place in the read/write interface (port))**, operable to output control signals along a control path of

said bus **(bus 100 in fig. 2) (col. 3, lines 5-40 discloses control channel to transfer data between a RAM and an I/O device, which take place in the bus)**, said control channel being operable to output said source control signal to said data source prior to receiving said received data at said read channel **(col. 3, lines 5-25 discloses control channel being operable to output said source control signal to said data source prior to receiving said received data at said read channel)**; and to generate a destination control signal specifying said at least one data transfer to said data destination **(col. 3, lines 5-25 discloses control channel being operable to output said data to destination)**, said control channel being operable to output said destination control signal to said data destination independently of whether said received data has been received at said read channel **(col. 1, lines 23-26 discloses "the DMA controller has two functions. In one function, the DMA controller causes the I/O device to output data and writes the data into the main storage. In the other function, the DMA controller reads out data from the main storage and causes the I/O device to receive the data")**..

9. As per **claims 15, 16, 30, and 31**, Minami discloses "wherein said at least one data transfer comprises a sequence of data transfers from a plurality of consecutive addresses **(col. 2, lines 16-34 discloses transfer from the source (RAM 120) to the plurality I/O devices and the other way around, where data is being transferred in a sequence from multiple I/O devices, where each of these I/O devices has an address)**, said control logic being operable to generate a single source or destination control signal to control sending or writing of said sequence of data transfers from said data source or destination" **(page 2 from the applicant's**

**specification sated "*Furthermore control logic in state machines are required to control the sequencing of the transfer of data from the source to the FIFO and from the FIFO to the destination*". Similarly, Minami discloses "In a case where data transfer is made while performing hand shaking using the two signals Req* and Ack* between the DMA controller and the I/O device in the above-stated manner, the data transfer rate obtainable by a perfect-synchronized-type design can be suppressed at the most to a transfer rate of "(I/O bus width).times.(system clock signal frequency).times.1/2", which is a control logic to transfer data between the source and the destination; see col. 3, lines 25-32. Combination of the Req* and Ack* signals are combined together for transfer control).**

## VI. RELEVANT ART CITED BY THE EXAMINER

10. The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See **MPEP 707.05(c)**.

11. The following references teach a DMAC for transfer data between a source and a data destination.

**U.S. PATENT NUMBER**

US 2002/0026543

US 5,594,923

## VII. CLOSING COMMENTS

***Conclusion***

**a. STATUS OF CLAIMS IN THE APPLICATION**

12. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

**a(1) CLAIMS REJECTED IN THE APPLICATION**

13. Per the instant office action, claims 13-16, and 28-31 have received a final action on the merits.

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

**b. DIRECTION OF FUTURE CORRESPONDENCES**

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ernest Unelus whose telephone number is (571) 272-8596. The examiner can normally be reached on Monday to Friday 9:00 AM to 5:00 PM.

## IMPORTANT NOTE

15. If attempts to reach the above noted Examiner by telephone is unsuccessful, the Examiner's supervisor, Mr. Fritz M. Fleming, can be reached at the following telephone number: Area Code (571) 272-4145.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

December 04, 2006

Ernest Unelus
Examiner
Art Unit 2181

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12/6/2006